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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,853	LEE, JU-IL	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 7-13* is/are rejected.

7)☐ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 9/1/06 has been entered.

Claim Objections

2. Claim 5 is objected to because of the following informalities: No immediately discernible antecedent basis for "the first and second gate insulator layers" in lines 18-19. There are no antecedent insulator layers in the claim. The term appears to be referring back to the previously introduced first and second gate insulators. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

It is possible Applicant intends the amended phrasing, "a stacked insulator having the first and the second gate insulator layers stacked thereon," to require the step (f) of forming the second gate insulator (which may be of identical composition to the first gate insulator) to form said second gate insulator in a way that allows it to retain a separate character from, and be stacked on, the first gate insulator. Assuming claim 5 must be construed in said fashion claims 5-13 are rejected under 35 U.S.C. 112, first

paragraph, as failing to comply with the written description requirement. Under said construction the claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The application as filed merely discloses "forming" second gate insulator on top of the first gate insulator, in the broadest sense of the term "forming." Amongst the specific ways to perform such a step known to the art, one way to form an oxide layer on top of another oxide layer formed on top of a silicon layer is the "second thermal oxidation" step described by Cagnina et al. 6,362,049. When a second layer is formed by thermal oxidation on top of a first layer previously formed by thermal oxidation, it is often difficult, after the step is performed, to discern a separate character by which the second layer may be distinguished from the first[1]. Applicant discloses no alternative way to perform this step (a way that might result in the second gate insulator retaining a separate identity after the process is complete). Therefore Applicant's specification does not describe this step in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of a process that results in a second gate insulator formed over a first gate insulator in a

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[1] Notwithstanding this difficulty, one can tell the step of forming the second layer has been performed, because the two layers, together, are thicker than the one layer that existed before performance of the second-layer-forming step.

"stacked" fashion, with the two gate insulators being separately discernible as elements of said stack, as is apparently claimed by the amended language of claim 5.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 5,12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over RHODES (6,333,205) in view of EL GAMAL ET AL. (6,642,543), CAGNINA ET AL. (6,362,049), and YANG ET AL. (6,184,055).

Rhodes discloses a method for manufacturing a CMOS image sensor, comprising the steps of a) preparing a semiconductor substrate 310 incorporating therein a p-type epitaxial layer (note paragraph 0041) therein, wherein the semiconductor substrate 310 is divided into two parts of which one part is defined as a pixel array 14 having a number of pixels, each pixel containing a drive transistor 36, a select transistor 38, a transfer transistor 29 and a reset transistor 31, and the other part is defined as a logic circuit 60, the pixel array 14 being isolated from the logic circuit 60 by means of a field oxide region 341 therebetween; f) forming a second gate insulator layer 315 in the pixel array 14 and a top face of the p-type epitaxial layer in the logic circuit 60; and g) forming a plurality of photodiodes 24 and a plurality of the drive transistors 36, the select

transistors 38, the transfer transistors 29 and the reset transistors 31 in the pixel array 14 based on the second gate insulator layer 315, and h) forming at least one transistor in the logic circuit 60 based on the second gate insulator layer 315. Note figures 1,2,4-17, column 3 lines 15-25, and column 7 lines 25-45 of Rhodes. Note that the examiner explicitly finds that Rhodes discloses a method for manufacturing a perfectly useful CMOS image sensor comprising each and every element recited in Applicant's steps a), f), g) (with one exception, discussed below) and h). A fuller sense of the examiner's findings of what Rhodes et al. discloses may perhaps be had by examining Rhodes' claims (noting that Rhodes published more than one year prior to applicant's application) 28-36. The examiner specifically finds that Rhodes' claims 28-36 each "read on" any conceivable embodiment of the invention of claim 5. That is to say, each and every element Rhodes claims, Applicant likewise claims in claim 5.

Rhodes does not, however, disclose that step f) should include forming the second gate insulator layer on top of a first gate insulator layer, that step g) should include an added step of basing the plurality of the drive transistors 36, the select transistors 38, the transfer transistors 29 and the reset transistors 31 in the pixel array 14 on said first gate insulator layer, or the steps of b) forming said first gate insulator layer of SiO_2 on a top face of the p-type epitaxial layer by thermally oxidizing the p-type epitaxial layer; c) forming a mask on a top face of the first gate insulator layer in the pixel array; d) removing the first gate insulator layer in the logic circuit by using the mask; and e) removing the mask in the pixel array using a thinner. Further, Rhodes does not disclose

that each transistor of the pixel array has a stacked insulator layer having the first and the second gate insulator layers stacked thereon.

However, El Gamal et al. discloses a CMOS image sensor with a pixel array 570 having thick (double-gate) gate insulators and a logic circuit 540-550 having thin gate insulators. At column 5 lines 22-25 El Gamal et al. explain that the thicker gate insulators in the pixel array allow the pixels to have higher dynamic range (i.e., the camera containing the pixel array produces brighter brights and darker darks). El Gamal et al. supplies no method whatsoever for producing thicker gate oxides in the pixel array. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. This is not a fatal flaw, enablement-wise, for El Gamal et al.'s patent, however. Prior to El Gamal et al.'s invention Cagnina et al. disclosed a method of producing thicker and thinner gate oxides comprising b) a step (see figure 3-106(a)) of forming an SiO_2 first gate insulator 701 on a top face of a p-type epitaxial layer 702 by thermally oxidizing the p-type epitaxial layer 702; c) a step (see figure 3-106(b)) of forming a mask (resist) 703 on a top face of the first gate insulator 701; d) a step of removing the first gate insulator 701 in the logic circuit by using the mask 703; e) a step of removing the mask 703 in the pixel array using a thinner; and a modification of Rhode's step of forming the second gate insulator 705, comprising (see figure 3-106(c)) forming the second gate insulator 705 on the top face of the first gate insulator 701 in a first circuit and a top face of the p-type epitaxial layer 702 in a second circuit; and basing first (high threshold voltage) transistors on the first and second gate insulator 705 layers while basing a second (low

threshold voltage) transistor on only the second gate insulator 705 layer. Note figures 3-106(a), (b), and (c), and column 5 lines 24-36 of Cagnina et al. Further, Yang et al. disclose a highly efficient method for forming a CMOS image sensor, wherein all the drive transistors, the select transistors, the transfer transistors and the reset transistors of a pixel are identical. It was Yang et al.'s discovery that the fastest and cheapest way to make drive transistors D_x, select transistors S_x, transfer transistors T_x and reset transistors R_x of pixel 713 was to first simultaneously form each of the gate insulators 711 of said transistors, each identically to its fellows, then to simultaneously and identically form all the gates 710 of said transistors, then to simultaneously and identically form all the sidewalls 726, then to simultaneously and identically form all the diffusions 729. Note figures 7E-7I and column 8 lines 7-64 of Yang et al. Yang and his illustrious co-workers thus suggested to one of skill in the art that that the most efficient way to apply El Gamal's teaching of using thicker gate insulators in the pixel region to obtain greater dynamic range to Rhodes' CMOS imager would be to simultaneously and identically form said thicker gate insulators in the al of the plurality of the drive transistors, the select transistors, the transfer transistors, and the reset transistors of said pixel region. Therefore, it would have been obvious to a person having skill in the art to augment Rhodes's method for manufacturing a CMOS image sensor with the steps of b) forming an SiO_2 first gate insulator on a top face of the p-type epitaxial layer by thermally oxidizing the p-type epitaxial layer; c) forming a mask (resist) on a top face of the first gate insulator in the pixel array; d) removing the first gate insulator in the

logic circuit by using the mask; e) removing the mask in the pixel array using a thinner; and forming the second gate insulator on the top face of the first gate insulator in the pixel array and a top face of the p-type epitaxial layer in the logic circuit; and supplying each of the drive transistors, the select transistors, the transfer transistors, and the reset transistors in the pixel with a stacked insulator layer having the first and the second gate insulator layers stacked thereon while basing a logic transistor on only the second gate insulator layer, such as disclosed by Cagnina et al. and Yang et al., and suggested by El Gamal et al., in order to allow the pixels to have higher dynamic range to thus provide a camera containing the pixel array with brighter brights and darker darks.

B. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over RHODES (6,333,205) in view of EL GAMAL ET AL. (6,642,543), CAGNINA ET AL. (6,362,049), and YANG ET AL. (6,184,055), as applied to claim 5 above, and further in view of AHN (5,804,491).

Rhodes, El Gamal et al., Cagnina et al., and Yang et al. suggest a method for manufacturing a CMOS image sensor with all the limitations of claims 7-9 except a step of removing a gate insulator by wet-etching with HF or BOE. Note figures 1,2,4-17, column 3 lines 15-25, and column 7 lines 25-45 of Rhodes. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. Note figures 3-106(a), (b), and (c), and column 5 lines 24-36 of Cagnina et al.

However, Ahn discloses a method for manufacturing with a step of removing a gate insulator by wet etching with HF or BOE. Note column 5 lines 28-31 of Ahn. Therefore, it

would have been obvious to a person having skill in the art to replace the thinner of Cagnina et al.'s step of removing a gate insulator with the HF or BOE such as taught by Ahn in order to quickly and fully remove the gate insulator to thus provide more efficient manufacture

C. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over RHODES (6,333,205) in view of EL GAMAL ET AL. (6,642,543), CAGNINA ET AL. (6,362,049), and YANG ET AL. (6,184,055), as applied to claim 5 above, and further in view of HORI ET AL. (5,707,487).

Rhodes, El Gamal et al., Cagnina et al., and Yang et al. suggest a method for manufacturing a CMOS image sensor with all the limitations of claims 7-9 except a step of removing a mask using sulfuric acid or an O_2 plasma etch. Note figures 1,2,4-17, column 3 lines 15-25, and column 7 lines 25-45 of Rhodes. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. Note figures 3-106(a), (b), and (c), and column 5 lines 24-36 of Cagnina et al.

However, Hori et al. discloses a method for manufacturing with a step of removing a mask using sulfuric acid or an O_2 plasma etch. Note column 2 lines 38-41 of Hori et al. Therefore, it would have been obvious to a person having skill in the art to replace Cagnina et al.'s step of removing a mask with the step of removing a mask using sulfuric acid or an O_2 plasma etch such as taught by Hori et al. in order to quickly and fully remove the mask to thus provide more efficient manufacture.

Allowable Subject Matter

5. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 5 and 7-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2826